

Interconnect Fabric Module

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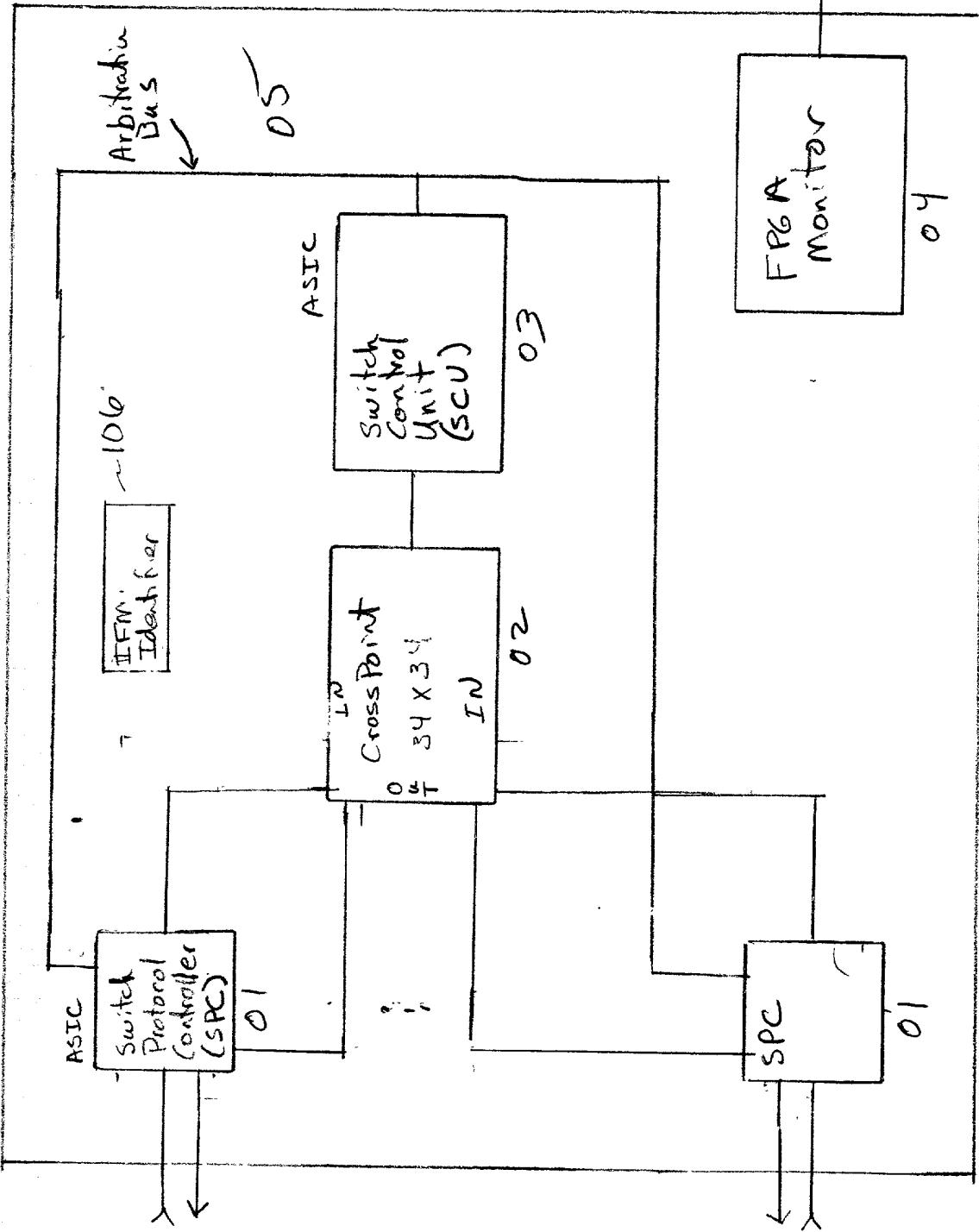


Fig 1

To/from crosspoint switch

Arbitration Bus

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Switch Protocol Controller (SPC)

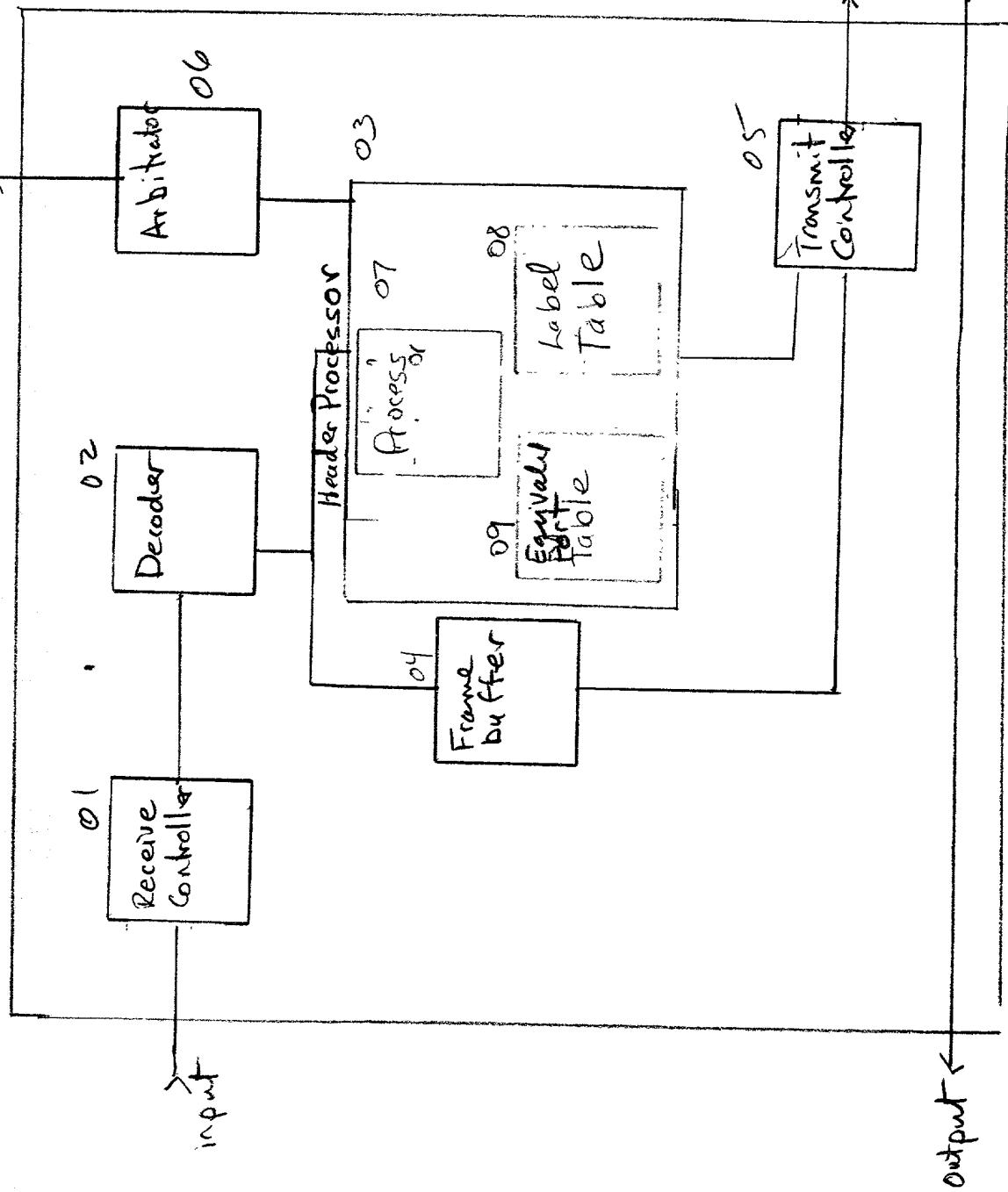


Fig 2

Label Table

The diagram illustrates a memory system architecture with the following components and mappings:

- Virtual Address:** The address is divided into three fields: **Port#**, **Page#,** and **Frame#.**
- Port Maps:** A table maps Port# to Page#.
- Page Table:** A table maps Page# to Frame#.
- Frame Table:** A table maps Frame# to Physical Address.

Specific values shown in the tables:

Port#	Page#
0	00
1	11
2	10

Page#	Frame#
00	00
01	01
10	00
11	01

Frame#	Physical Address
00	0000 0000 0000 0000
01	0000 0000 0000 0001

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M
S
L

Frame

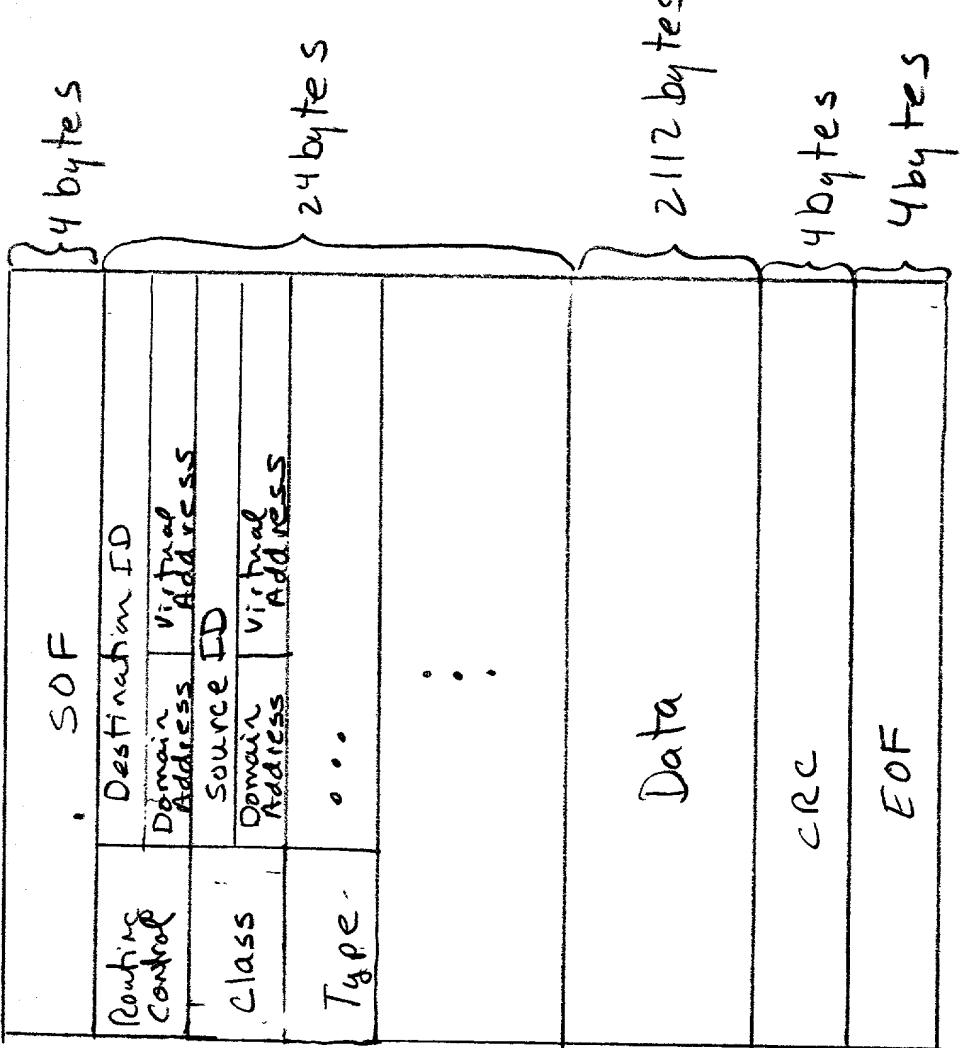


Fig 4

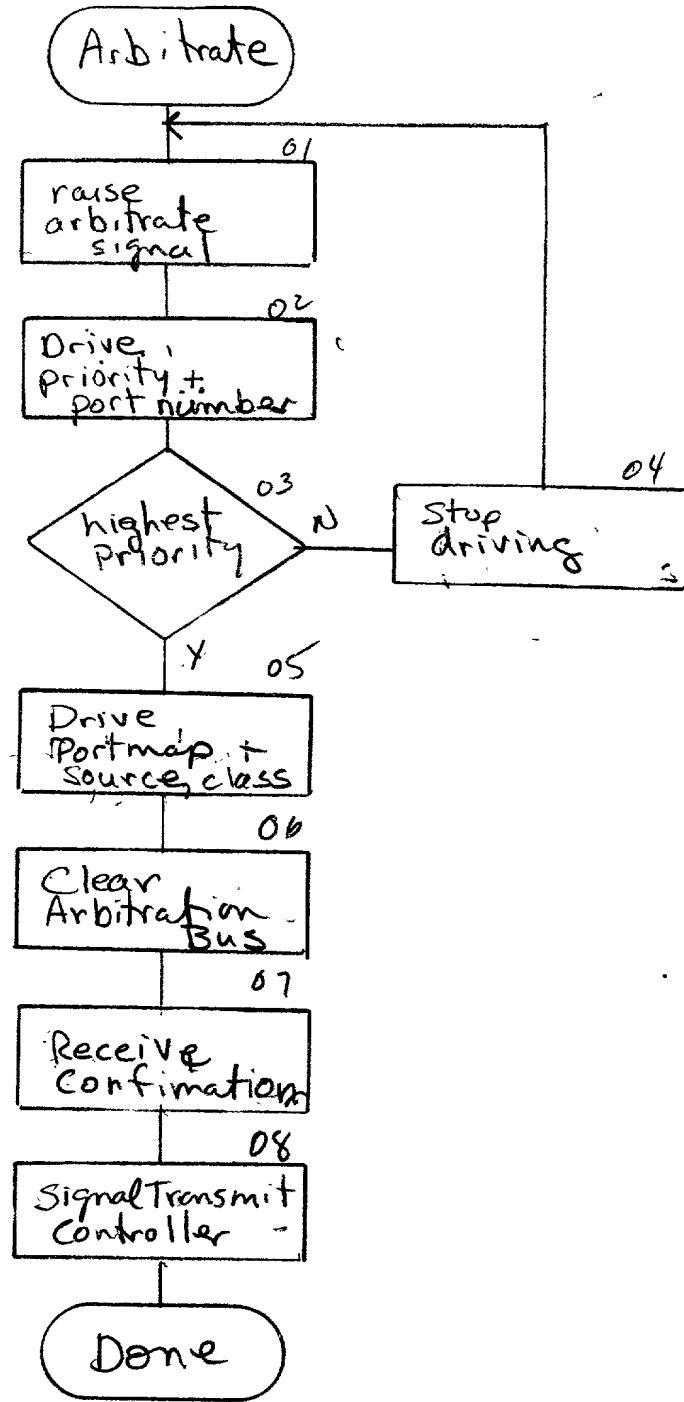


Fig 5

Transmission Controller

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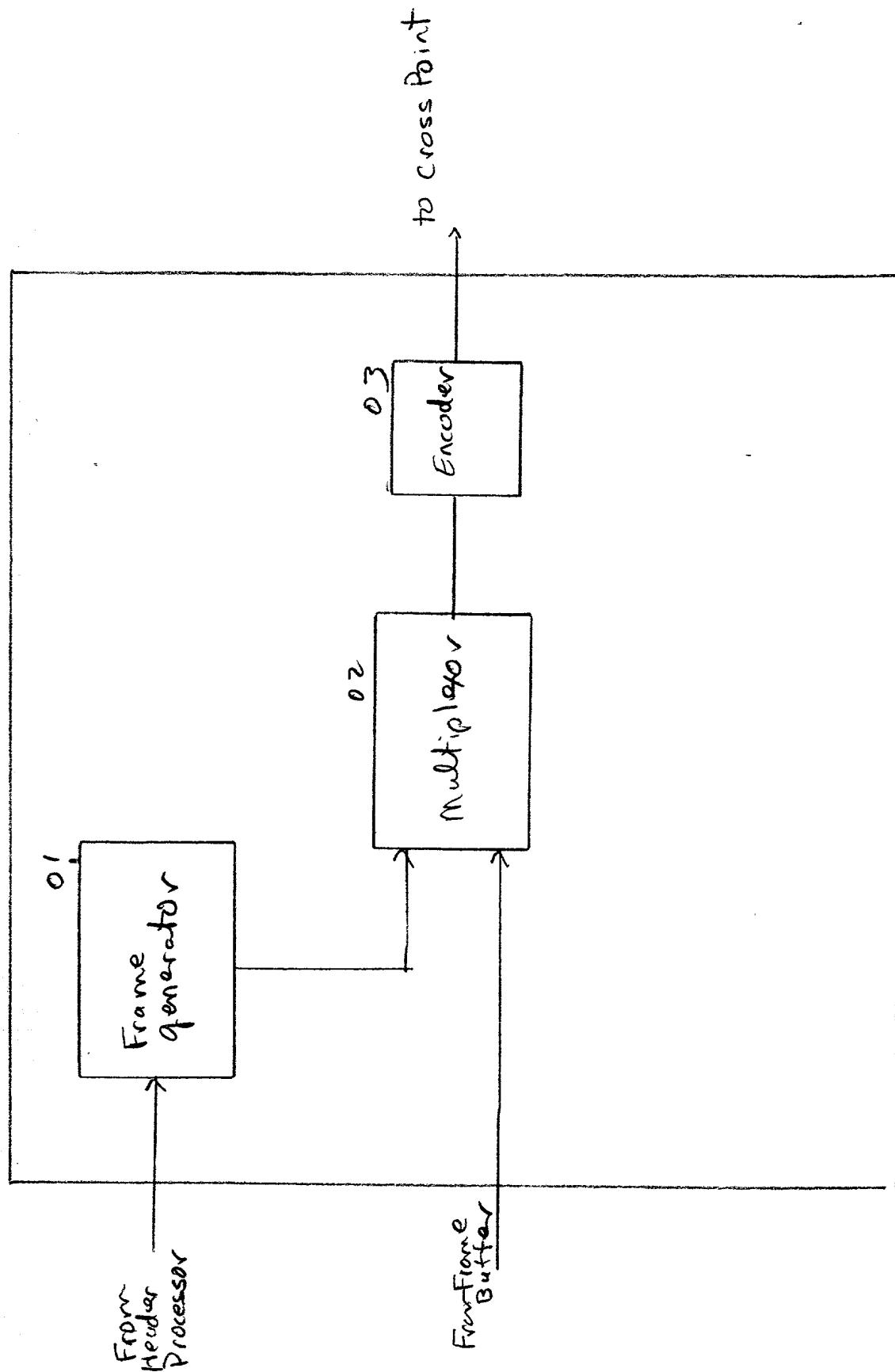


Fig 4

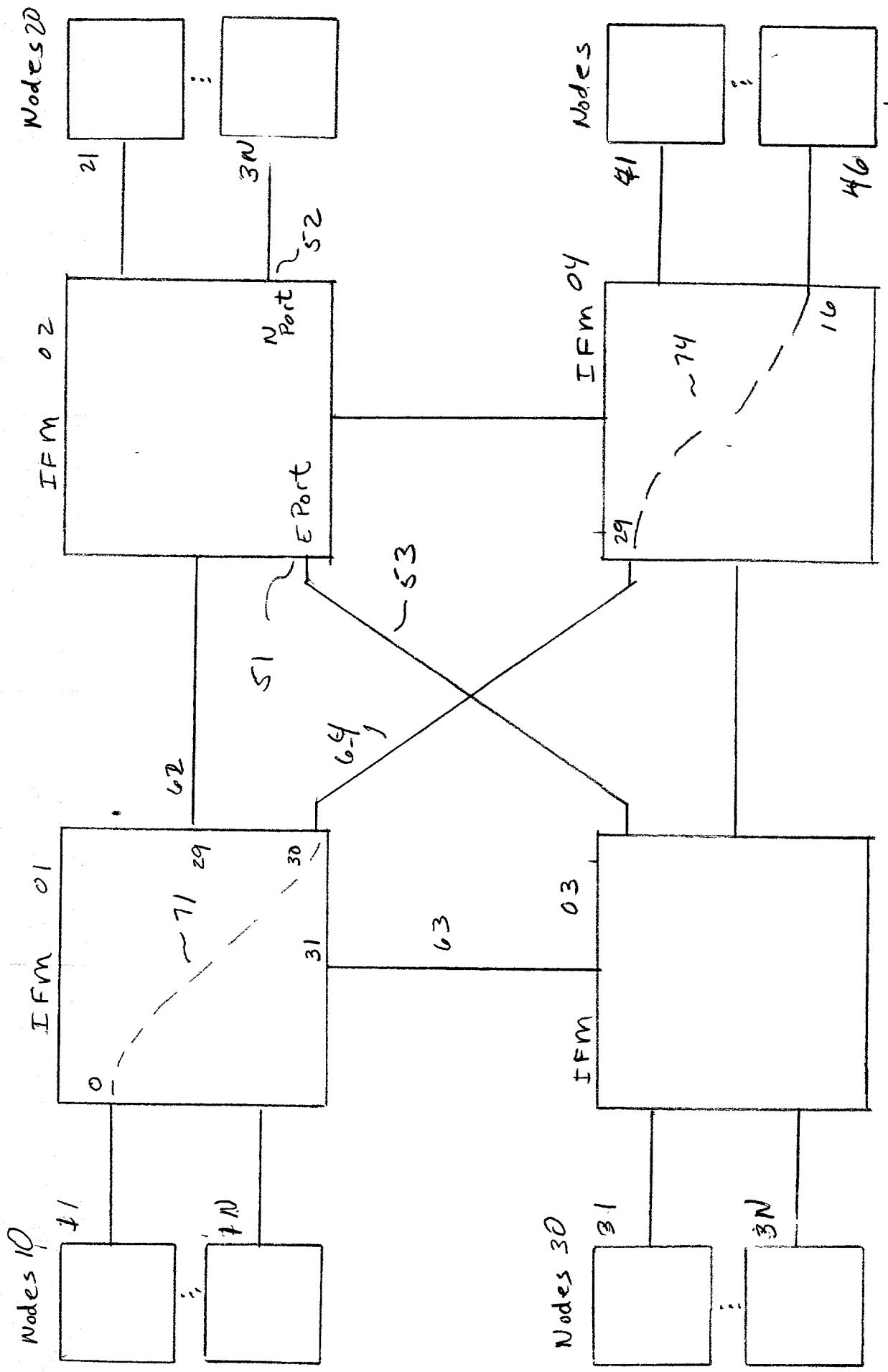


Fig 7

/ 42

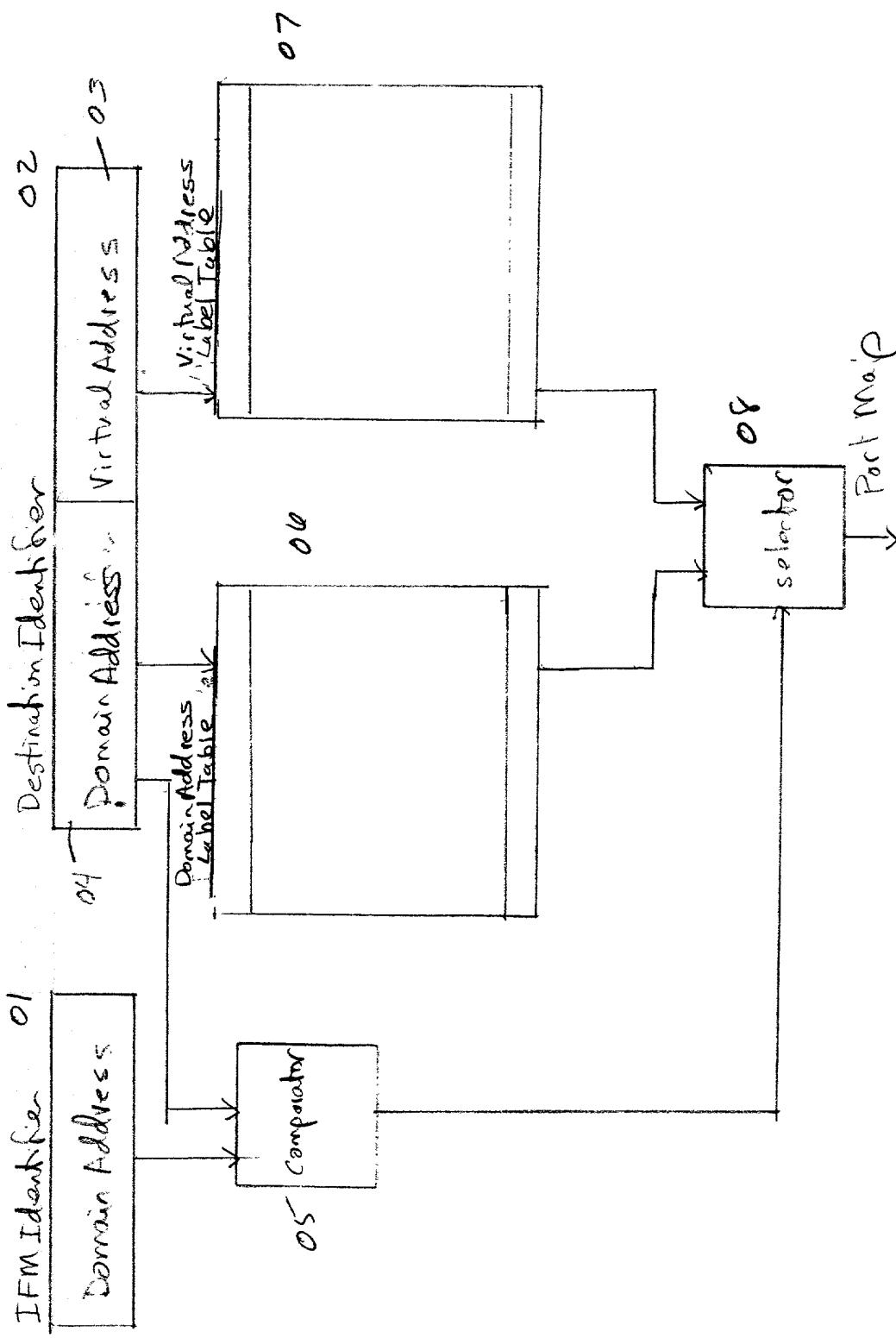


Fig. 8

Quad Switch Protocol Controller

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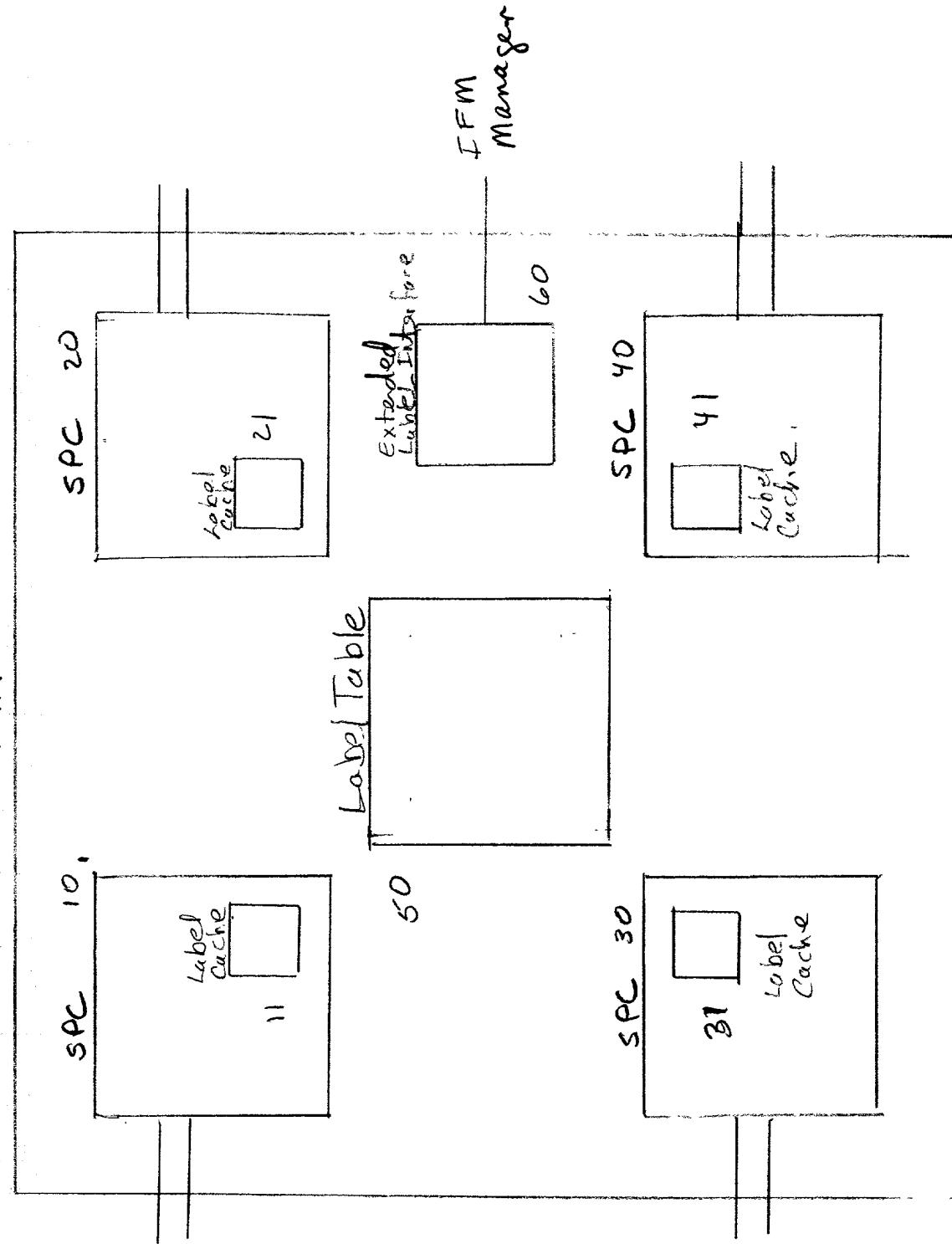
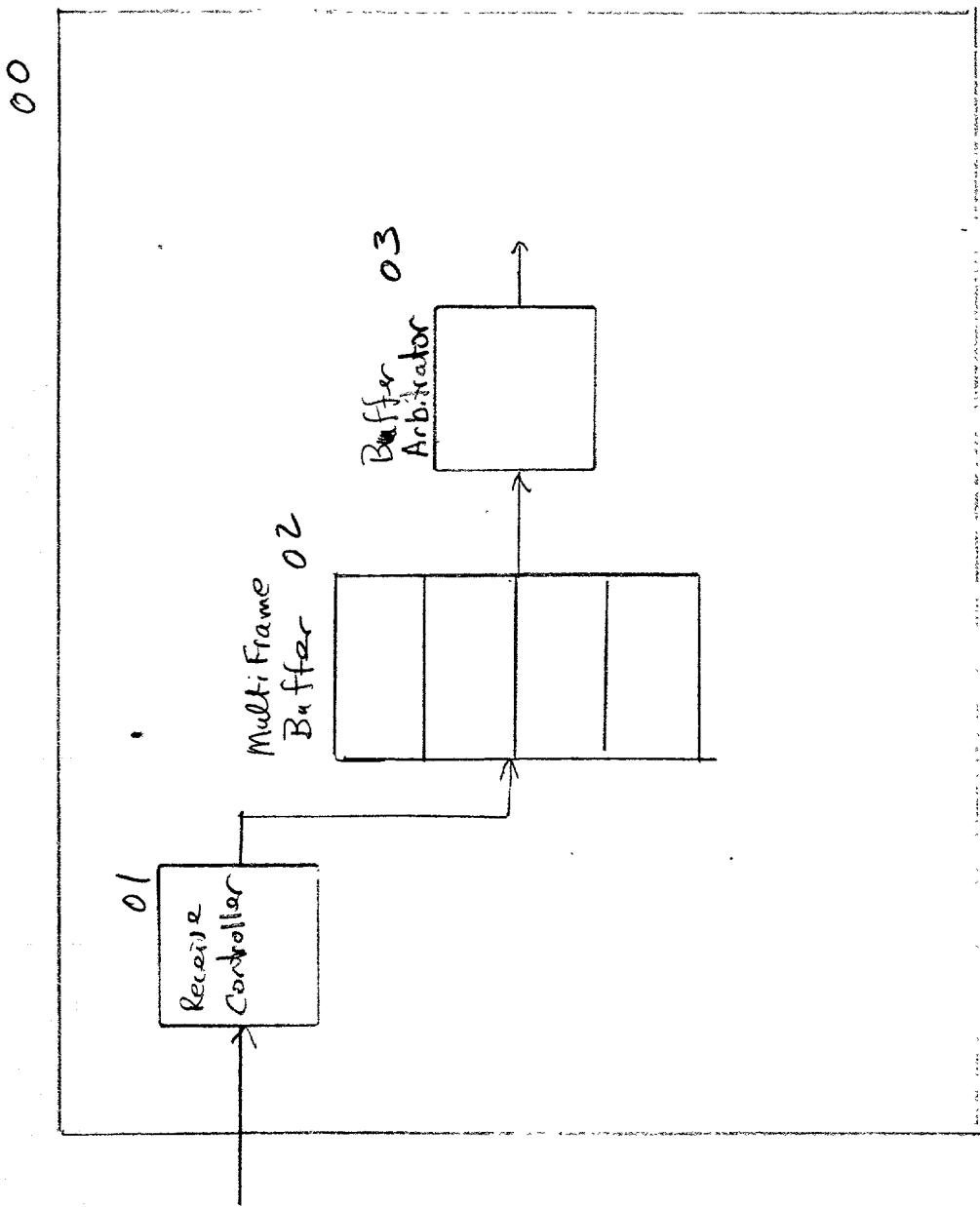


Fig 9

Fig 10



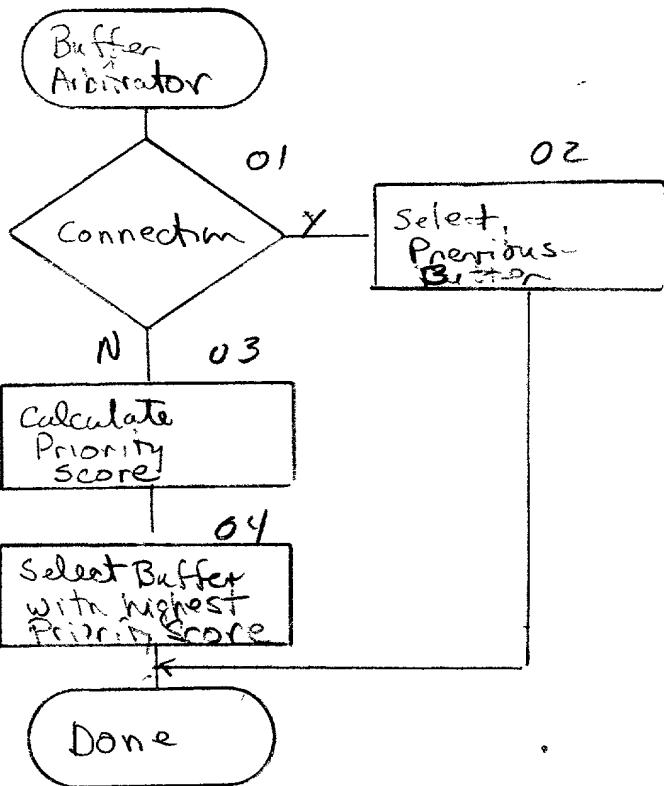
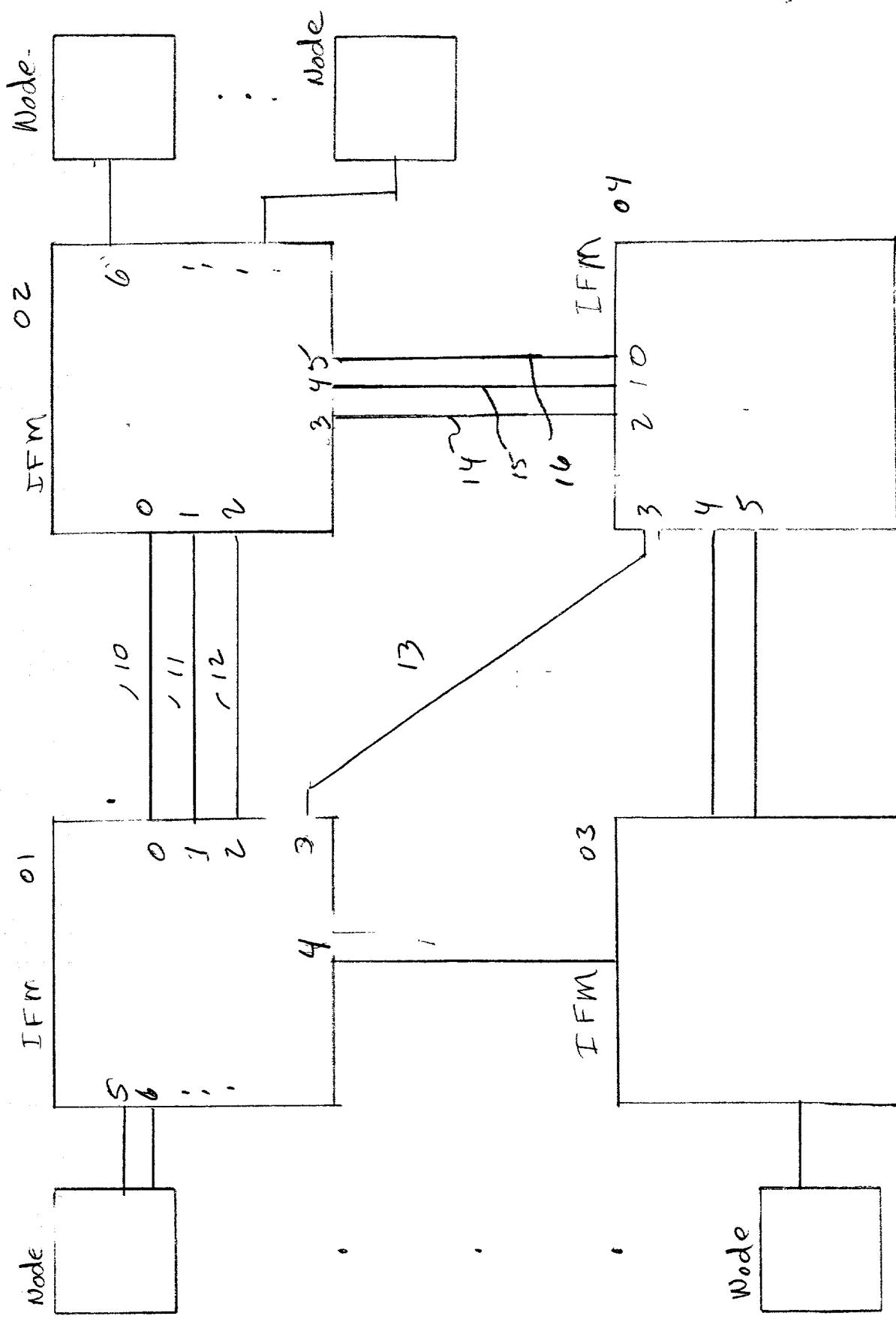


Fig 11

Fig 12



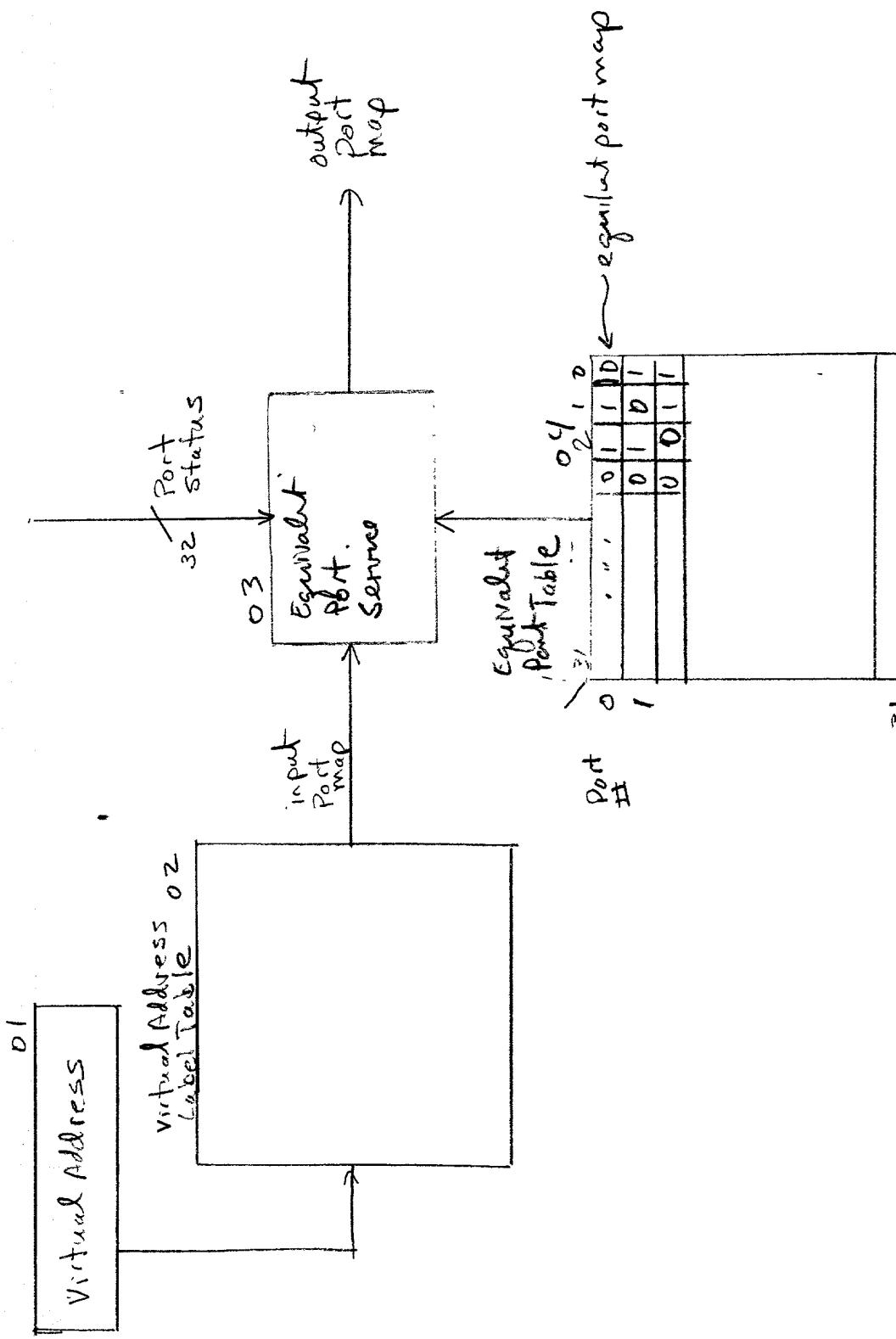


Fig 13

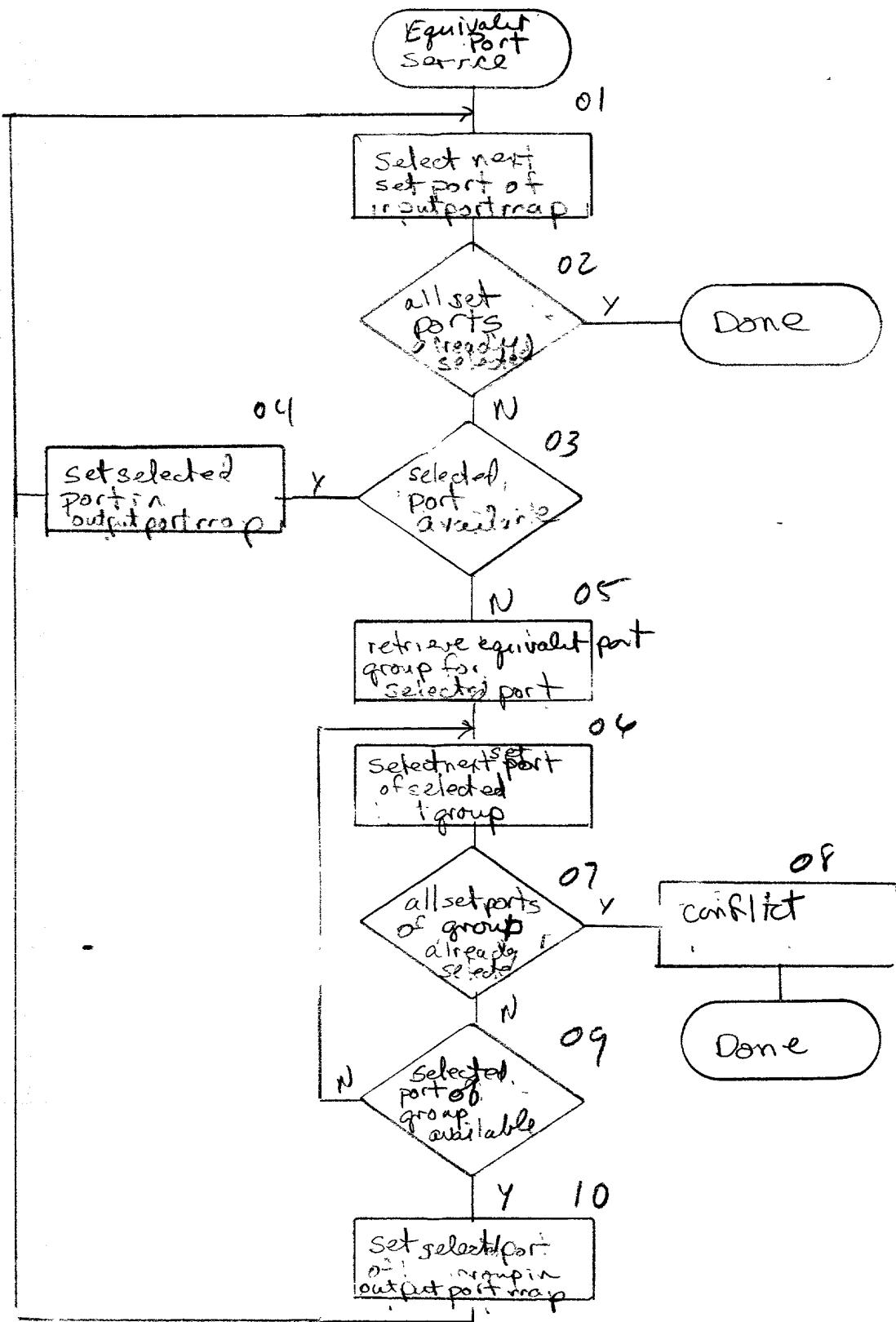


Fig 14

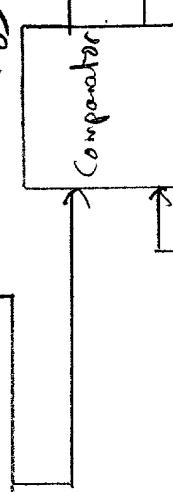
Header Processor

Forwarding & Segmentation

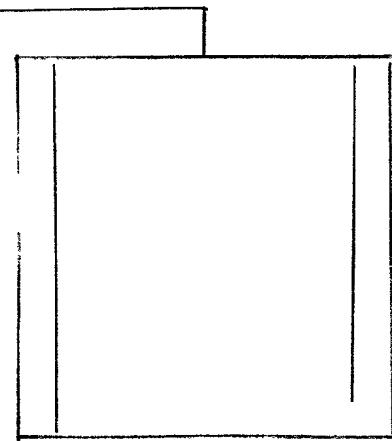
Destination Index

01 03

Virtual Address



Reserved
Virtual Address Table



enable port 32
enable port 33

IFM 0 5

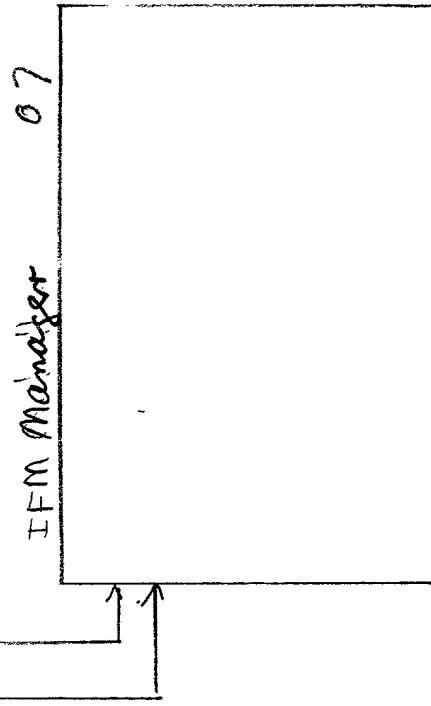
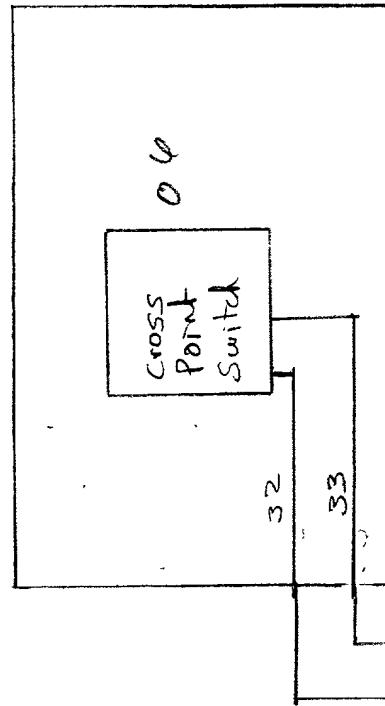
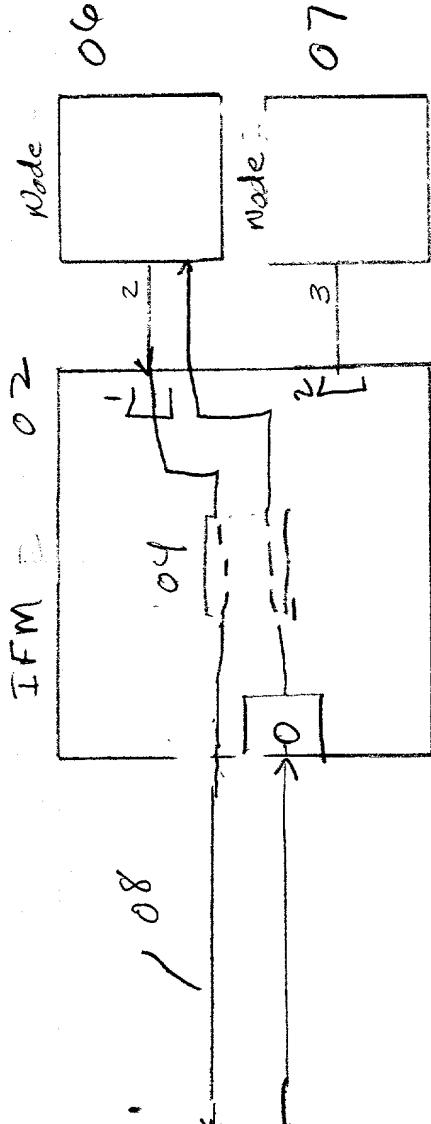
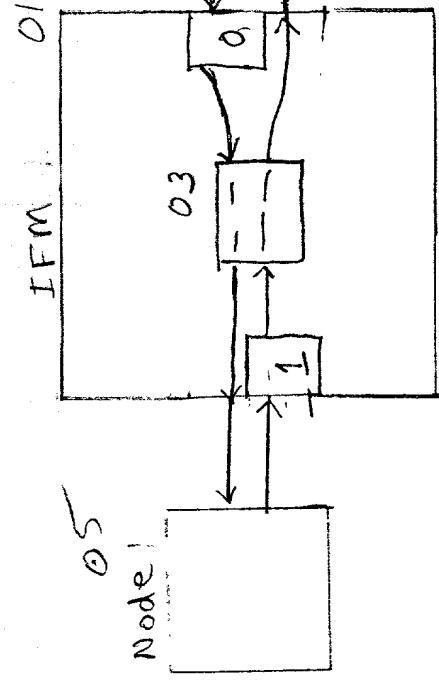


Fig 15



Dead lock

Time Node 1 uses I/F M 1601 Node 2 uses I/F M 1602
0 send start connect 1, 2

- | | | |
|---|------------------------------------|----------------------------------|
| 1 | connect
$1 \leftrightarrow 0$ | connect
$2 \leftrightarrow 0$ |
| 2 | Forward start connect | Forward start connect |
| 3 | can't forward start connect node 1 | can't forward start connect |

F18/16

Avoid
Contentlock

After end-to-end
is established

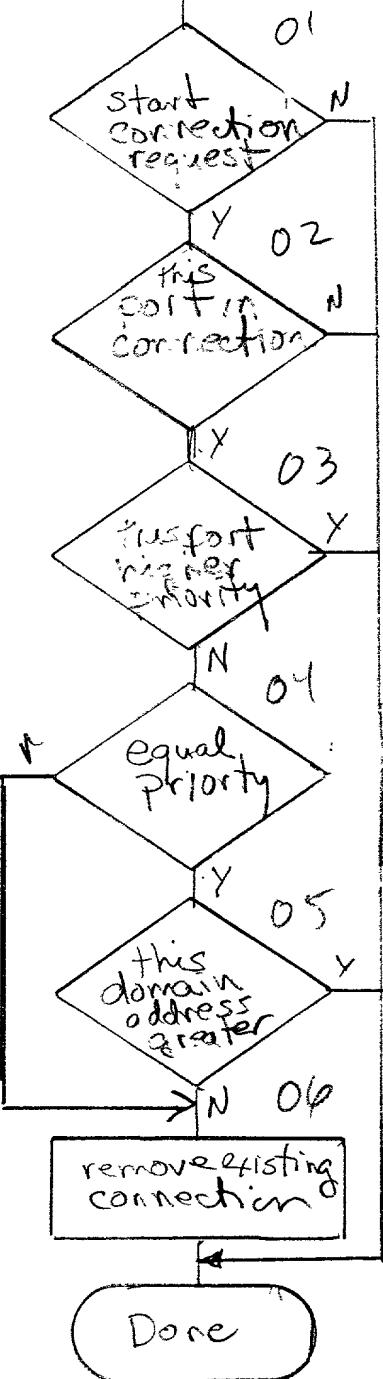
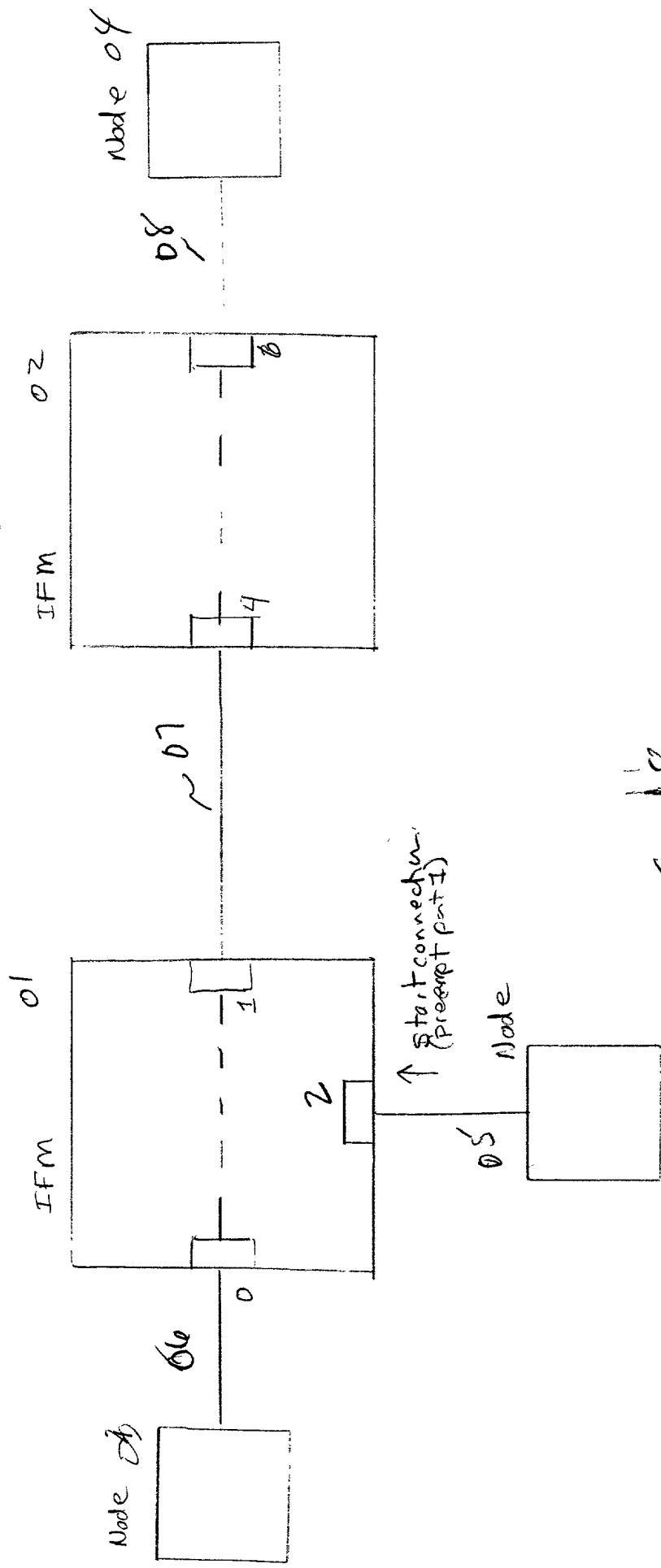


Fig 17

Fig 18



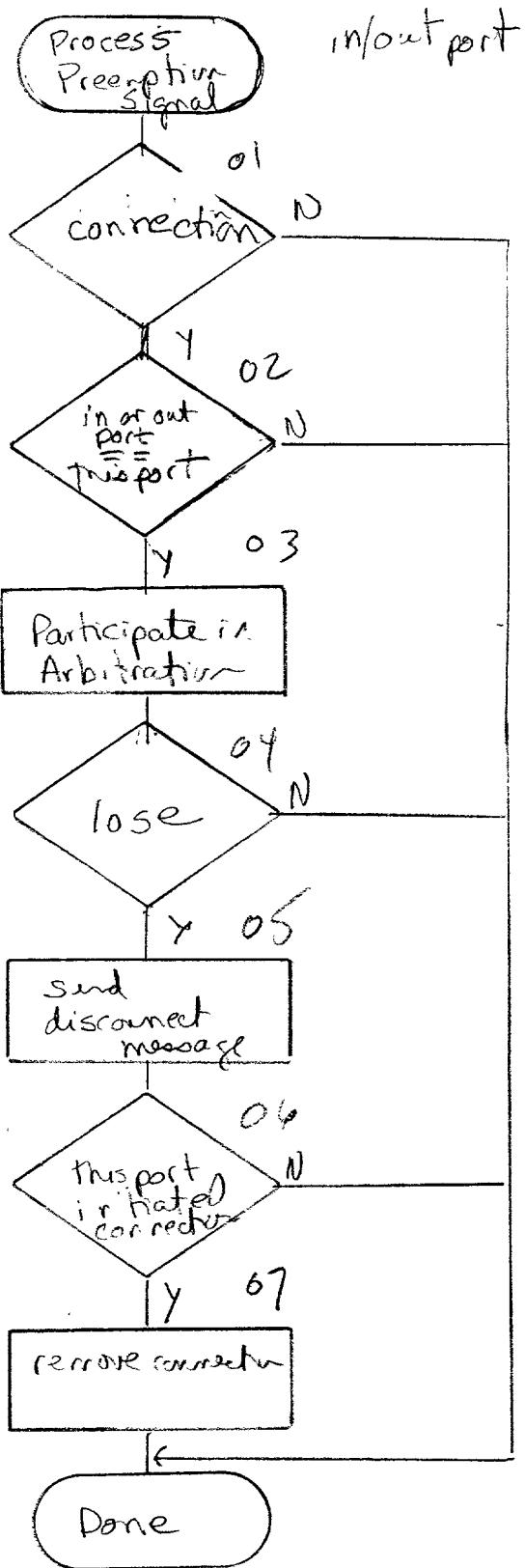


Fig. 19

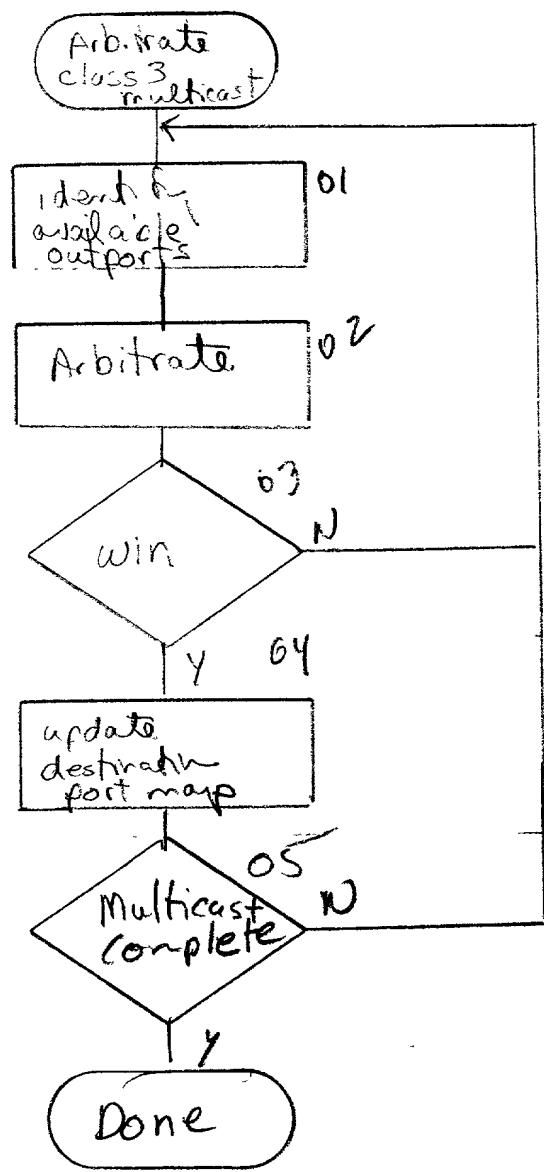


Figure 20